IN THE SPECIFICATION

Please replace the paragraph beginning at page 1, line24 with the following rewritten paragraph:

A1

--In such systems, the use of EPR4 Viterbi data detection techniques is widely used. EPR4 or EFPR4 Viterbi detectors are well known, and involve probabilistic techniques for determining data states in the data channel. As data rates increase in the data channel, it becomes increasingly difficult to distinguish adjacent data pulses, and the Viterbi techniques have been found to be very useful.--

Please replace the paragraph beginning at page 2, line 3 with the following rewritten paragraph:

A2

--Unfortunately, significant errors still occur in data detection. For example, using EPR4 techniques, a bit error rate (BER) of about 10^{-5} typically occurs. However it has been observed that if the signal to noise ratio in a system could be increased by, for example, only 1 dB, the bit error rate can be improved to 10^{-6}. This represents an order of magnitude improvement. Thus, even small improvements in the signal-to-noise ratio can result in large improvements in the bit error rate using EPR4 detection techniques. This is significant since presently the requirements exist for the provision of circuits that have a bit error rate less than 10^{-7}, and it is expected that this requirement will continue to become more stringent.—

Please replace the paragraph beginning at page 12, line 20 with the following rewritten paragraph:

A3

--The recovered write current is applied to a filter 37, which includes a series of delay elements 40 – 48 that delay the respective samples of the recovered write current at the outputs from the Viterbi 34, each for a delay time D. The delay time, D, corresponds to the sample period of the sampled data on the input line 32, and, as

A3 cont.

known, corresponds to a delay operator, equal to $e^{j\omega\Box}$, where w is frequency, and □ is delay time. The filter 37 may be an FIR filter, as shown. The inputs to the delay blocks 40, 41, 43, and 44 are multiplied by weighting factors 1, 2, -2, -1, respectively, and are summed by a summer circuit 50. The output from the summer 50 is a filtered output signal derived on the output line 51.--